

MULTILEVEL COPPER INTERCONNECT WITH DOUBLE PASSIVATION

Related Application(s)

5 This application is a Divisional of U.S. Application No. 09/584,157, filed May 31, 2000, which is incorporated herein by reference.

Technical Field

 This invention relates generally to integrated circuits and in particular to multilayer metal wiring interconnects in an integrated circuit assembly.

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Background of the Invention

 Integrated circuits, the key components in thousands of electronic and computer products, are interconnected networks of electrical components fabricated on a common foundation, or substrate. Fabricators typically use various techniques, such as layering, doping, masking, and etching, to build thousands and even millions of microscopic resistors, transistors, and other electrical components on a silicon substrate, known as a wafer. The components are then wired, or interconnected, together with aluminum wires to define a specific electric circuit, such as a computer memory. The aluminum wires are typically about one micron thick, or about 100 times thinner than a human hair.

 To form the aluminum wires, fabricators sometimes use a dual-damascene metallization technique, which takes its name from the ancient Damascene metalworking art of inlaying metal in grooves or channels to form ornamental patterns. The dual-damascene technique entails covering the components on a wafer with an insulative layer of silicon dioxide, etching small holes in the insulative layer to expose portions of the components underneath, and subsequently etching shallow trenches from hole to hole to define a wiring pattern.

 Etching the trenches and holes entails forming a mask, using photolithographic techniques, on the insulative layer. The masks, which typically consists of a

material called photoresist, shields some portions of the insulative layer from the etchant and allows the etchant to dissolve away other portions. After etching, fabricators remove the mask to expose the patterned insulative layer. They then blanket the entire insulative layer with a thin sheet of aluminum and polish off the excess, leaving behind aluminum vias, or contact plugs, in the holes and thin aluminum wires in the trenches.

The complexity of some integrated circuits demand several interconnected levels of wiring. Some circuits, such as microprocessors, have five or six interconnected levels, with each level formed by repeating the basic dual-damascene produce. For example, to form a second wiring level, fabricators apply a new insulative layer over the first wiring layer, form another mask on the new layer, etch holes and trenches into the new layer, remove the mask, blanket the new layer with aluminum, before finally polishing off the excess to complete it.

In recent years, researchers have begun using copper instead of aluminum to form integrated-circuit wiring, because copper offers lower electrical resistance and better reliability at smaller dimensions. Fabrication of copper-wired integrated circuits sometimes follows an extension of the dual-damascene method which includes an additional step of lining the holes and trenches of an insulative layer with a copper-diffusion barrier before blanketing the layer with copper and polishing off the excess. (The diffusion barrier is generally necessary because copper atoms readily diffuse through common insulators, such as silicon dioxide, resulting in unreliable or inoperative integrated circuits.) Typically, the copper-diffusion barrier is more than 30 nanometers thick and consists of tantalum, tantalum nitride, tantalum-silicon-nitride, titanium nitride, or tungsten nitride. Filling the barrier-lined holes and trenches with copper generally entails depositing a thin copper seed layer on the copper-diffusion barrier, electroplating copper on the seed layer, and then polishing off the excess.

The present inventors identified at least two problems with using the extended dual-damascene technique for making the copper wiring. The first is that typical

copper-diffusion barriers add appreciable resistance to the copper wiring, and thus negate some promised performance advantages. And, the second is that the number of separate procedures or steps necessary to make the copper wiring using the extended technique makes fabrication both costly and time consuming.

5 In a copending application by K. Y. Ahn and L. Forbes, entitled "Methods for Making Integrated-Circuit Wiring from Copper, Silver, Gold, and other Metals," application serial number 09/484303, an electroplated copper technology was disclosed. After fabrication of multilevel copper structure using sacrificial layers of photoresist, a very thin WSiN diffusion barrier was deposited on the copper air-
10 bridge structure by deposition of WSi by CVD, followed by ECR plasma nitridation. The space between the metal lines was then filled with a dielectric material of choice in one step. The WSiN layer thus formed serves to prevent the diffusion of copper into the dielectric material. Furthermore, any unreacted silicon can be converted to a very thin film of SiO₂ or Si₃N₄ in order to provide a substantial
15 amount of protection against electrochemical corrosion due to moisture and impurities in the dielectric layer.

The passivation bestowed by the extremely thin silicide/oxide or silicide/nitride layers formed above may prove to be quite sufficient for protecting the metal line air-bridge structures. On the other hand, the metal line air-bridge 101 is a three-
20 dimensional structure having a large surface area in the aggregate with very small spacings between its numerous top, bottom and side surfaces. Hence, it is possible that the silicide/(SiO₂ or Si₃N₄) barriers may contain a very small number of localized structural and chemical defects which could serve as corrosion nucleation centers.

25 Thus, even with the above described approaches, there is a need for yet improved structures and methods for multilevel Copper interconnects for ULSI circuits.

Summary of the Invention

The above mentioned problems associated with integrated circuit size and performance, the via and metal line formation process, and other problems are addressed by the present invention and will be understood by reading and studying
5 the following specification.

The structures and methods of the present invention include a method for forming multilevel wiring interconnects in an integrated circuit assembly. The method includes forming a number of multilayer metal lines separated by a number of air gaps above a substrate. A silicide layer is formed on the number of multilayer
10 metal lines. The silicide layer is oxidized. And, a low dielectric constant insulator is deposited to fill a number of interstices created by the number of air gaps between the number of multilayer metal lines. In one embodiment, forming the number of multilayer metal lines includes a first conductor bridge level. In one embodiment, forming a silicide layer on the number of multilayer metal lines includes using
15 pyrolysis of silane in the presence of a dopant source at a temperature of approximately 325 degrees Celsius. Also, in one embodiment, a metal layer is formed on the oxidized silicide layer. The metal layer includes a metal layer selected from the group consisting of Aluminum, Chromium, Titanium, and Zirconium. In one embodiment, the metal layer includes a layer of Aluminum oxide.

20 These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means
25 of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figures 1A-1D are cross sectional views of a fabrication embodiment for a multilevel wiring interconnect in an integrated circuit assembly according to the teachings of the present invention.

5 Figures 2A-2B illustrate another fabrication embodiment according to the teachings of the present invention.

Figure 3 illustrates a cross sectional view of an embodiment for a multilevel wiring interconnect in an integrated circuit assembly according to the teachings of the present invention.

10 Figure 4 illustrates a system having an integrated memory circuit and incorporating a multilevel wiring structure formed according to the teachings of the present invention.

Description of the Preferred Embodiments

15 In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to
20 include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in
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the art. The term conductor is understood to include semiconductors, and the term insulator is defined to include any material that is less electrically conductive than the materials referred to as conductors. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

The purpose of this invention is to disclose alternate methods, materials and processes for forming a diffusion barrier and additional overcoat(s) over the surface of a multilevel metal line air-bridge structure.

Figure 1A is a cross sectional view of a fabrication embodiment stage for a multilevel wiring interconnect in an integrated circuit assembly according to the teachings of the present invention. The structure shown in Figure 1A begins from the completion of a multilevel metal line air-bridge structure as disclosed in the commonly assigned U.S. Patent No. 5,891,797, entitled "Method of Forming a Support Structure for Air Bridge Wiring of an Integrated Circuit," issued April 6, 1999, the same is incorporated herein by reference. Figure 1A assumes that the multilevel metal line air-bridge has proper support structure as discussed in above referenced patent. Further, Figure 1A assumes that not only does the multilevel metal line air bridge have proper support, including posts if necessary, but also that design rules are used to avoid areas shadowed by wide metal lines and maximize open spaces in the 3-D structure. An example of the same is disclosed in copending, commonly assigned applications U.S. serial numbers 09/488098 and 09/484303, the same of which are incorporated herein. To achieve the same, those cases mention the manner in which wide metal lines are replaced by individual narrow lines connected in electrical parallels.

As shown in Figure 1A, the cross sectional view of a multilevel metal line wiring structure 101 includes a number of metal line levels. The embodiment shown in Figure 1A has a first metal line, second metal line, and third metal line levels, 102, 104 and 106 respectively. In Figure 1A, a first level metal line 108 is

represented as continuous metal line 108 running in a direction parallel to the plane of the drawing page in the first metal line level 102. As shown in Figure 1A, first metal line 108 is separated by an air gap in this portion the cross sectional view from a substrate 100. As one of ordinary skill in the art will understand upon reading the following disclosure the substrate 100 can include one or more transistors, or semiconductor structures/devices represented as 103A and 103B in Figure 1A. In Figure 1A, second metal line level 104 shows a number of second level metal lines 110-1, 110-2, . . . , 110-N which are represented running in a direction perpendicular to the plane of the drawing page. In the cross sectional view of Figure 1A, the number of second level metal lines 110-1, 110-2, . . . , 110-N are separated from the first level metal line 108 by an air gap in this portion of the cross sectional view. In Figure 1A, third metal line level 106 shows a third level metal line 112 which is represented as a continuous metal line 112 running in a direction parallel to the plane of the drawing page. As shown in Figure 1A, third level metal line 112 is separated in this portion of the cross sectional view by an air gap from the number of second level metal lines 110-1, 110-2, . . . , 110-N. One of ordinary skill in the art will understand, upon reading this disclosure, that the embodiment shown in Figure 1A is only one cross hatched configuration for multilevel metal lines in a multilayer semiconductor circuit. Other metallization circuit design are similarly included in the scope of the present invention.

One of ordinary skill in the art will understand from studying this disclosure together with commonly assigned U.S. Patent No. 5,891,797, the manner in which the number of multilevel, or multilayer, metal lines can be interconnected between the multilevels to complete electrical connection. The same is not described in more detail in connection with the embodiment of Figure 1A so as not to obscure the invention. Figure 1A thus represents one starting point for the multilevel, or multilayer, metallization structure of the present invention. From this starting point, a more detailed description of the present invention's fabrication process proceeds.

Figure 1B is an exploded view of a cross section of one of the number of second level metal lines 110-1, 110-2, . . . , 110-N. The exploded view of second level metal line, e.g. second level metal line 110-N, is useful in illustrating, in more detail, the wiring interconnects structure in a subsequent fabrication stage according to the teachings of the present invention. As one of ordinary skill in the art will understand upon reading this disclosure, the subsequently discussed process steps equally apply to and occur on each metal line separated by air gaps in the various metal line levels, e.g. 102, 104 and 106. In one embodiment, each of the metal lines separated by air gaps in the various metal line levels, 102, 104, and 106 in Figure 1A, include a metal line selected from the group consisting of Aluminum, Copper, Silver, and Gold. As shown in Figure 1B, according to the teachings of the present invention, a thin layer of silicide 114 is formed by exposing the metal line structure to a diluted silane mixture. This includes forming the thin layer of silicide using pyrolysis of silane in the presence of a dopant source. In one embodiment, exposing the metal line structure to a diluted silane mixture includes exposing the metal lines using a method similar to that disclosed in an article by A. L. Cabrera et al., entitled "Oxidation Protection for a Variety of Transition Metals and Copper via Surface Silicides formed with Silane Containing Atmosphere," J. Mater. Res., 6, no. 1, p. 71-79 (1991), and/or in an article by S. Hymes et al., entitled "Passivation of Copper by Silicide Formation in dilute Silane," MRS Conf. Proceedings, ULSI-VII, p. 425-431 (1992). The initial work by Cabrera et al. found that copper silicone coatings were formed at a temperature as low as 350°C when copper is exposed to a gaseous ambient containing a small concentration (typically <2%) of silane. The silicided copper surface was found to be substantially resistant to electrochemical and atmospheric corrosion. Hymes et al. then did a more systematic research of copper silicidation. Short periods of low temperature (325°C) exposure to silane produced barely detectable amounts (by RBS) of silicon on the copper surface. However, even these few monolayers of silicide (most likely present as the gamma phase) led to an improvement in the copper corrosion resistance.

Figure 1C illustrates the structure following the next sequence of processing steps. As shown in the exploded view of Figure 1C, the silicide layer 114 can be either oxidized or undergo a nitridation process to create either a silicon dioxide (SiO_2) or a silicon nitride (Si_3N_4) layer 116. The passivation bestowed by the extremely thin silicide/oxide or silicide/nitride layers 116 formed above may prove to be quite sufficient for protecting the metal line air-bridge structures 101 shown in Figure 1A. On the other hand, the metal line air-bridge 101 is a three-dimensional structure having a large surface area in the aggregate with very small spacings between its numerous top, bottom and side surfaces. Hence, it is possible that the silicide/(SiO_2 or Si_3N_4) barriers, e.g. 114 and 116, may contain a very small number of localized structural and chemical defects which could serve as corrosion nucleation centers. Thus, the present invention also teaches processes and materials for further enhancing the reliability of the hermetic sealing of the metal line air-bridge structure 101.

According to one embodiment of the present invention, the silicide/(SiO_2 or Si_3N_4) barriers, e.g. 114 and 116, are deposited onto the metal line air-bridge structure 101 by the following method. That is, in Figure 1B a very thin silicide layer 114 is formed on the number of metal lines by exposing the metal lines to a dilute silane ambient at 325°C for several minutes. At this relatively low temperature, the inner portion of the silicon layer 114 will react with the metal line to form an extremely thin intermetallic layer of silicide 114. In the embodiment where the number of metal lines are Copper, the inner portion of the silicon layer 114 will react with the metal line to form an extremely thin intermetallic layer of Copper silicide 114. The formation of this compound will serve as a barrier to the continued diffusion of Cu and/or Si and further growth of the silicide phase. Next, as shown in Figure 1C, most or all of the remaining, unreacted silicon in the outer region will then be converted to: a SiO_2 layer 116 by thermal or plasma anodization in an oxygen plasma; or, to a Si_3N_4 layer 116 in a nitrogen plasma. Although only a

few atomic layers thick, the additional oxide or nitride passivating layer 116 will provide improved hermetic sealing of the underlying copper.

As shown in Figure 1D, a low dielectric constant insulator 118 can then be deposited in a single step to fill a number of interstices created by the air gaps
5 between the surfaces of the number of multilayer metal lines. As one of ordinary skill in the art will understand upon reading this disclosure, a final CMP step can be used to planarize the structure and remove the insulating oxide (or nitride) and the metal, e.g. Copper, silicide barrier from the top surfaces of the uppermost contact pads of the metal line air-bridge structure 101. Wide latitude can be used in
10 selecting this low dielectric constant insulator 118, e.g. filling polymer, since the hermetic encapsulation is known to be a highly effective barrier that will prevent the transport of ions, molecules and moisture across it. In the absence of such a perfect hermetic barrier, transport of various moieties could serve to induce a number of undesirable events including: localized copper corrosion and ultimate failure of the
15 air-bridge; and, long-term polarization of the polymeric filler material 118 which could lead to the development of unacceptably large, localized fringing fields which would unpredictably interfere with the proper functioning of an underlying transistor array, number of semiconductor devices, e.g. 103A and 103B, and associated circuits in the substrate 100.

20 An extension of the above approach is to deposit a much thicker silicide layer 114 at a somewhat higher temperature (e.g., in the 300 to 500°C range) and convert some or all of this to a thicker oxide or nitride protective layer 116. This embodiment is shown in Figure 1D in which it can be noted that the SiO_2 or Si_3N_4 layer 116 occupies a significant portion of the spaces, or number of interstices,
25 between adjacent levels of the multilayer metal line structure. In addition to providing even a higher degree of hermetic encapsulation, the use of an appreciably thicker silicon dioxide or silicon nitride encapsulant 116 will provide substantial mechanical strengthening of the metal line air-bridge structure. As one of ordinary skill in the art will understand upon reading this disclosure, the achievable

strengthening will depend on the relative thicknesses of the overcoat(s), e.g. layer 116, to the number of metal lines, e.g. copper, as well as the cross-sectional configurations, or circuit layout, of the multilayer metal line air-bridge components. Due to the well-known brittleness of silicon dioxide and silicon nitride when
5 subjected to tensile and/or bending forces, no attempt is made here to quantify the extent of the overcoat(s)/copper structures.

Figure 2A illustrates yet another embodiment which expands the possibilities inherent in the present invention. In the embodiment shown in Figure 2A, the method of the present invention continues from the structure shown in Figure 1C. In
10 Figure 2A, a subsequent metal layer 220 is deposited on the SiO_2 or Si_3N_4 layer 216. According to the teachings of the present invention, the metal layer 220 includes a metal layer 220 selected from the group consisting of Aluminum, Chromium, Titanium, and Zirconium. For example, in one embodiment a metal layer of Aluminum 220 is deposited by a low pressure chemical vapor deposition (LPCVD)
15 process on the multilayer metal line air-bridge structure following the addition and oxidation (or, nitridization) of the thicker silicide layer, e.g. layers 214 and 216. The structure is now as shown in Figure 2A.

In Figure 2B, the Aluminum layer 220 is then partially or totally converted to Aluminum oxide represented by layer 224. The Aluminum layer 220 is partially or
20 totally converted to Aluminum oxide layer 224 by oxidation in an oxygen-containing ambient or by the well-known process of anodic oxidation in an oxygen plasma. As one of ordinary skill in the art will understand upon reading this disclosure, the number of other vacuum-deposited metals including chromium, titanium and zirconium, as stated above, can similarly be used in place of Aluminum
25 according to the steps described herein.

As one of ordinary skill in the art will understand upon reading this disclosure, the metal layer 220 according to the teachings of the present invention further offers the advantage of being "self passivating." As known in the art, corrosion is an electrochemical process requiring at least several monolayers of water (serving as an

electrolyte) in contact with metal. Water in solution in a polymer or other dielectric cannot serve as an electrolyte. However, there may be pockets underneath the metallization incompletely filled with polymer. Water pockets might collect in such places. If this occurs, corrosion can be accelerated where two dissimilar metals are
5 in contact. This acceleration can be large when a reactive metal, e.g. high on the Electromotive Force Scale (EMF), contacts a more noble metal lying towards the bottom of the EMF scale. The difference in their EMF's generates an electrical potential causing dissolution of the reactive metal. aluminum, titanium, and chromium lie high on this scale while copper is near the bottom. In spite of the
10 EMF differences, however, corrosion is not accelerated here because of another factor. Aluminum, titanium, and chromium can extract oxygen from water to form extremely effective passivating oxide barriers which protect these metals from corrosion, even in the presence of copper or gold, etc. Hence the origin of the phrase "self-passivating." Incidentally, niobium, hafnium, and vanadium and a few
15 other metals exhibit self-passivation as well.

Deposition of Silicon on the Multilayer Metal Lines

The following descriptive methods are provided as various method embodiments for creating the environment to form a silicide layer 114 according to
20 the teachings of the present invention. Polysilicon is generally deposited by pyrolysis of silane in the temperature range of 580-650°C by using low-pressure chemical vapor deposition (LPCVD). Good thickness uniformity, high purity and high throughput can be achieved by this process. The structure and properties of the polysilicon films depend very much upon the deposition temperature, dopant type
25 and concentration and subsequent thermal cycling. Films deposited below 580°C are essentially amorphous. Above this temperature, one obtains polycrystalline films having preferred orientations: a {111} fiber axis with columnar grains is dominant near 625°C and a {100} texture near 675°C as disclosed in an article by T.

I. Kamins, entitled "Structure/properties of LPCVD Si Films," J. Electrochem. Soc., 127, 686 (March, 1980).

Deposition temperatures noted in the above LPCVD process, however, may be too high for applications in back-end processing which favor lower temperature processes. Accordingly, it is noted that the present invention can be performed at lower processing temperatures. To illustrate the same, reference is made to a silicon deposition process described by H. Keppner et al., in an article entitled "The Micromorph Cell: A New Way to High-Efficiency Low-Temperature Crystalline Thin-Film Cell Manufacturing," MRS Symposium Proc., 452, p. 865-876 (1996).

10 The same is incorporated herein by reference. In this article, Keppner et al. demonstrated successful deposition of microcrystalline silicon films at temperature as low as 220°C for applications in solar cells. In one embodiment, the same process can be used according to the teachings of the present invention for forming a silicide layer 114 on the multilayer metal line structure 101. Utilizing a very high
15 frequency glow-discharge technique (VHF-GD) at 70 MHZ in a parallel plate reactor, deposition rates up to 9.4 Å/s are attainable using mixtures of silane, hydrogen, and argon. Further, it has been shown that it is possible to grow polycrystalline silicon thin films by hot-wire CVD (HW CVD) at a relatively low temperature of 430°C for photovoltaic applications by varying the hydrogen dilution
20 of the silane feedstock gas, the gas pressure, and the wire temperature. The same is described in an article by J. K. Rath et al., entitled "Low-Temperature Deposition of Polycrystalline Silicon Thin Films by Hot-Wire CVD," Solar Energy Materials and Solar Cells, 48, p. 269-277 (1997) which is incorporated herein by reference. Other researchers have reported the growth of amorphous silicon films in the 30-120° C
25 range, and polycrystalline films at temperatures as low as 120°C using an electron cyclotron resonance (ECR PECVD) system. The same is described in an article by S. Bae et al., entitled "Low-Temperature Deposition Pathways to Silicon Nitride, Amorphous Silicon, Polycrystalline Silicon and n-type Amorphous Silicon Films Using a High Density Plasma System," IEEE Conf. Record - Abstract, International

Conference on Plasma Science, p. 315 (1997) which is incorporated herein by reference. It has also been shown that an ECR PECVD system can be used to deposit polycrystalline silicon thin films at room temperature and 500°C. The same is described in an article by Y. C. Jeon and S.-W. Lee, entitled "Low Temperature
5 Fabrication of Polycrystalline Silicon Thin Films by ECR CVD," Electrochem. Soc. Proceedings, 94, no. 35, p. 103-104 (1995) which is incorporated herein by reference. The use of ECR CVD for the growth of polycrystalline silicon films with micro-meter-order grains at 250°C has also been described in an article by K.-C. Wang et al., entitled "Very Low Temperature Deposition of Polycrystalline Silicon
10 Films with Micrometer Order Grains on SiO₂," MRS Symposium Proceedings, 335, p. 582-586 (1995). The same is incorporated herein by reference. One of ordinary skill in the art will understand upon reading this disclosure, that any one or a number of the above referenced processes can be used to deposit a silicon layer on the number of metal lines from which to form the silicide layer 114 in the multilayer
15 metal line structure according to the teachings of the present invention. These processes are disclosed in connection with the present invention as illustrative embodiments of the manner in which the present invention may be performed. The scope of the present invention, however, is not so limited. One of ordinary skill in the art will appreciate other suitable methods for forming a silicide layer 114 on the
20 number of metal lines of the present invention as part of forming the novel multilevel wiring interconnects of the present invention.

Oxidation of Silicon

The following descriptive methods are provided as various method
25 embodiments for forming the oxide layer or oxidized silicon layer for one structural embodiment of the present invention. In general, lightly-doped polySi oxidizes more rapidly in wet oxygen than single crystal silicon. Polysilicon heavily doped with phosphorous oxidizes more rapidly than undoped polySi. Thus, according to one embodiment of the present invention, forming the silicide layer 114 on the

number of metal lines includes using pyrolysis of silane in a temperature range of between 300 to 500 degrees Celsius in the presence of a dopant source to achieve a lightly doped silicide layer 114 on the number of metal lines. Another embodiment includes using pyrolysis of silane in a temperature range of between 300 to 500
5 degrees Celsius in the presence of a dopant source to achieve a heavily doped silicide layer 114 on the number of metal lines. In one such embodiment, the heavily doped silicide layer 114 includes a silicide layer 114 which is heavily doped with phosphorous. The ratio of polySi consumed during oxidation to the thickness of oxide is approximately 1:1.56.

10 Again, it is noted that the present invention can be performed at low processing temperatures for applications where low thermal budget is critical. In such applications a low-temperature oxidation process such as magnetically excited plasma oxidation can be used. A low-temperature oxidation process is described in an article by Y. Okamoto et al., entitled "Magnetically Excited Plasma
15 Oxynitridation of Si at Room Temperature," Japan. J. Apply. Phys., 34, Part 2, no. 8A, pp. L995-957 (1995) and is incorporated herein by reference. Another combined plasma and rapid-thermal processing approach is described in an article by S. V. Hattangaday et al., entitled "Integrated Processing of Silicon Oxynitride Films by Combined Plasma and Rapid-thermal Processing," J. Vac. Sci. Technol., A
20 14(6), p. 3017-23 (1996). This article is similarly incorporated herein by reference. It is further noted that a microwave plasma discharge at very low temperatures, e.g. at 200 to 250°C, has been used for the growth of thin silicon oxynitride films suitable for gate dielectric applications. The addition of CHF₃ as a source of fluorine enhanced the growth rate as described in an article by S. K. Ray et al.,
25 entitled "Fluorine-enhanced Nitridation of silicon at Low Temperatures in a Microwave Plasma," J. Apply. Phys., 70, no. 3, p. 1874-6 (1991) which is incorporated herein by reference.

These processes for oxidation of silicon are disclosed in connection with the present invention as illustrative embodiments of the manner in which the present

invention may be performed. The scope of the present invention, however, is not so limited. One of ordinary skill in the art will appreciate other suitable methods for oxidizing silicon to form the oxidized silicon layer 116 of the present invention as part of forming the novel multilevel wiring interconnects of the present invention.

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Nitridation of Silicon

The following descriptive methods are provided as various method embodiments for forming the nitride layer or nitrided silicon layer for one structural embodiment of the present invention. It is much more difficult to form Si_3N_4 than SiO_2 as outlined in an article by S. Dushman and J. M. Lafferty, entitled "Scientific Foundations of Vacuum Technique, 2nd Edition," John Wiley and Sons (1962). Although solid silicon will not react noticeably with N_2 and/or NH_3 below approximately 1000°C , it will react with radicals and neutrals formed in plasmas containing these gases at much lower temperatures. This is described in an article by G. B. Kistiakowsky and G. G. Volpi, in J. Chem. Phys., 27, 1141 (1957); and by H. F. Winters et al., in an article entitled "Influence of Surface Adsorption Characteristics on Reactively Sputtered Films Grown in the Biased and Unbiased Modes," J. Appl. Phys., 43, No. 3, 794-799 (1958) which are incorporated herein by reference. Relatively thin layers (approximately 50 to 200 angstroms) of Si_3N_4 can be grown by reacting a N_2 or NH_3 plasma with silicon at temperatures below 200°C as described in an article by T. Keyser et al., entitled "Low Temperature Plasma Nitridation Process and Application of Nitride Films Formed Thereby," and U.S. Patent 4,762,728, issued August 9, 1988 which are incorporated herein by reference.

Growth rates of Si_3N_4 are faster in NH_3 than in N_2 plasmas. For the purpose of the present invention, silicon can be converted to a Si_3N_4 passivation layer 116 by heating to temperatures in the 200 to 400°C range in the presence of a NH_3 plasma. Control of the silicon nitride thickness can be accomplished by suitable manipulation of such variables as temperature, gas pressure and substrate bias. These processes for nitridation of silicon are disclosed in connection with the

present invention as illustrative embodiments of the manner in which the present invention may be performed. The scope of the present invention, however, is not so limited. One of ordinary skill in the art will appreciate other suitable methods for the nitridation of silicon to form the nitrided silicon layer 116 of the present

5 invention as part of forming the novel multilevel wiring interconnects of the present invention.

Deposition of a Metal Layer, e.g. Aluminum, on SiO₂ or Si₃N₄

Conformal coatings of a metal layer 220 on the SiO₂ or Si₃N₄ layer 216 of the
10 present invention can be formed by LPCVD processes using a number of reactants and conditions. For example, conformal coatings of Aluminum can be formed by LPCVD as disclosed in an article by J. L. Vossen and W. Kern, entitled "Thin Film Processes. II," Academic Press, Inc. (1991) which is incorporated herein by reference. Also, LPCVD Aluminum films from trimethylamine complexes of alane
15 as precursors have been investigated in detail and were found to yield mirror finish Aluminum films at reasonable rates at temperatures as low as 180°C in a hot walled system. The same is described in an article by W. L. Gladfelter et al., entitled "Chemistry of Materials 1," 339 (1989) which is incorporated by reference. These processes are disclosed in connection with the present invention as illustrative
20 embodiments of the manner in which the present invention may be performed. The scope of the present invention, however, is not so limited. One of ordinary skill in the art will appreciate other suitable methods for depositing a metal layer 220, including a metal layer selected from the group consisting of Aluminum, Chromium, Titanium, and Zirconium, on the SiO₂ or Si₃N₄ layer 216 of the present invention as
25 part of forming the novel multilevel wiring interconnects of the present invention.

Oxidation of Metal Layers, e.g. Aluminum

The following descriptive methods are provided as various method embodiments for oxidizing metal layers for one structural embodiment of the

present invention. In particular the descriptive method present here is that for oxidation of an Aluminum metal layer. However, one of ordinary skill in the art will understand, upon reading this disclosure, the manner in which similar oxidation techniques can be performed to oxidize a metal layer, including a metal layer
5 selected from the group consisting of Aluminum, Chromium, Titanium, and Zirconium in order to create the oxidized metal layer 224 of the present invention as part of forming the novel multilevel wiring interconnects of the present invention. Thermal oxidation of aluminum proceeds slowly, forming approximately 25 angstroms of oxide in about 2 hours at 100°C in one atmosphere of oxygen as
10 described in an article by J. Grimblot and J. M. Eldridge, entitled "II. Oxidation of Aluminum Films," J. Electrochem., 129, 2369 (1982). The same is incorporated herein by reference. The addition of large concentrations of water vapor to the reacting ambient increases the oxidation rate by perhaps 50% or so. The amorphous Aluminum Oxide (Al_2O_3) grown in either oxygen or steam is extremely dense,
15 coherent and inert in most environments and thus has outstanding passivating properties. In cases like this, the passivation is bestowed by the quality of the surface oxide, not its thickness. As but one example of this principle, the atmospheric corrosion rate of permalloy ($\text{Fe}_{0.80}\text{Ni}_{0.20}$) can be increased by 100-fold by introducing defects and impurities into the approximately 20 angstrom,
20 passivating layer of Fe_2O_3 that forms when this alloy is exposed to the ambient atmosphere. The same is disclosed in an article by J. M. Eldridge, entitled "New Approaches For Investigating Corrosion in Thin Film Devices," Electronic Packaging and Corrosion in Microelectronics, ASM (1987) and incorporated herein by reference. Thus, according to the teachings of the present invention, the
25 oxidation of the metal layer is performed to avoid the introduction of defects and impurities such that the oxidized metal layer is essentially defect and impurity free.

Again, these processes are disclosed in connection with the present invention as illustrative embodiments of the manner in which the present invention may be performed. The scope of the present invention, however, is not so limited. One of

ordinary skill in the art will appreciate other suitable methods for oxidizing a metal layer 220, including a metal layer 220 selected from the group consisting of Aluminum, Chromium, Titanium, and Zirconium, to produce one embodiment of the novel multilevel wiring interconnects of the present invention.

5 Figure 3 illustrates a cross sectional view of an embodiment for an integrated memory circuit including a multilevel wiring interconnect in an integrated circuit assembly according to the teachings of the present invention. As shown in Figure 3, the multilevel wiring interconnect in an integrated circuit assembly includes a metal line air-bridge structure as disclosed in the commonly assigned U.S. Patent
10 No. 5,891,797, entitled "Method of Forming a Support Structure for Air Bridge Wiring of an Integrated Circuit," issued April 6, 1999, the same is incorporated herein by reference. In Figure 3, the cross sectional view of a multilevel metal line wiring structure 301 includes a number of metal line levels. The embodiment shown in Figure 3 has a first metal line, second metal line, and third metal line
15 levels, 302, 304 and 306 respectively, each containing a number of metal lines. In Figure 3, a first level metal line 308 is represented as continuous metal line 308 running in a direction parallel to the plane of the drawing page in the first metal line level 302. As shown in Figure 3, first metal line 308 is separated by an air gap in this portion the cross sectional view from a substrate 300. As one of ordinary skill
20 in the art the substrate 300 can include one or more transistors, or semiconductor structures/devices which are represented by 303A and 303B in Figure 3. One of ordinary skill in the art will further appreciate that a number of metal lines, such as metal line 108, connect to the one or more transistors, or semiconductor structures/devices 303A and 303B in a manner as disclosed in commonly assigned
25 U.S. Patent No. 5,891,797, entitled "Method of Forming a Support Structure for Air Bridge Wiring of an Integrated Circuit," issued April 6, 1999. In one embodiment, the metal line 108 includes a first conductor bridge level. In Figure 3, second metal line level 304 shows a number of second level metal lines 310-1, 310-2, . . . , 310-N which are represented running in a direction perpendicular to the plane of the

drawing page. In Figure 3, third metal line level 306 shows a third level metal line 312 which is represented as a continuous metal line 312 running in a direction parallel to the plane of the drawing page. One of ordinary skill in the art will understand, upon reading this disclosure, that the embodiment shown in Figure 3 is only one cross hatched configuration for multilevel metal lines in a multilayer semiconductor circuit. Other metallization circuit designs are similarly included in the scope of the present invention.

One of ordinary skill in the art will understand from studying this disclosure together with commonly assigned U.S. Patent No. 5,891,797, the manner in which the number of multilevel, or multilayer, metal lines can be interconnected between the multilevels to complete electrical connection. The same is not described in more detail in connection with the embodiment of Figure 3 so as not to obscure the invention. According to one embodiment of the present invention, each of the metal lines selected from the group consisting of Aluminum, Copper, Silver, and Gold.

As shown in Figure 3, according to the teachings of the present invention, a thin silicide layer 314 is formed on the number of second level metal lines 310-1, 310-2, . . . , 310-N. A layer of silicon dioxide or silicon nitride, e.g. SiO_2 or Si_3N_4 , 316 is formed on the silicide layer 314 on the number of second level metal lines 310-1, 310-2, . . . , 310-N.

As shown in Figure 3, a subsequent metal layer 320 is formed on the SiO_2 or Si_3N_4 layer 316. According to the teachings of the present invention, the metal layer 320 includes a metal layer 320 selected from the group consisting of Aluminum, Chromium, Titanium, and Zirconium. In Figure 3, the metal layer 320 includes a metal oxide layer 324.

Finally, as shown in Figure 3, a low dielectric constant insulator 318 fills a number of interstices between the surfaces of the number of multilayer metal lines. Wide latitude can be used in selecting this low dielectric constant insulator 318, e.g. filling polymer, since the hermetic encapsulation is known to be a highly effective barrier that will prevent the transport of ions, molecules and moisture across it. In

the absence of such a perfect hermetic barrier according to the teachings of the present invention, transport of various moieties could serve to induce a number of undesirable events including: localized copper corrosion and ultimate failure of the air-bridge; and, long-term polarization of the polymeric filler material 318 which could lead to the development of unacceptably large, localized fringing fields which would unpredictably interfere with the proper functioning of an underlying transistor array, number of semiconductor devices, e.g. 303A and 303B, and associated circuits in the substrate 300.

Figure 4 illustrates a system 400 having an integrated memory circuit 430 and incorporating a multilevel wiring structure formed according to the teachings of the present invention. As one of ordinary skill in the art will understand upon reading this disclosure, this system 400 includes a processor 410 and an integrated circuit, or integrated memory circuit 430 coupled to the processor 410. The processor 410 can be coupled to the integrated memory circuit 430 via any suitable bus 420, as the same are known and understood by one of ordinary skill in the art. In the embodiment, the processor 410 and integrated circuit 430 are located on a single wafer or die. Again, at least a portion of the integrated circuit 430 includes a multilevel wiring structure as disclosed in the various embodiments provided herein.

Conclusion

Thus, the present invention provides structures, systems and methods for multilevel wiring interconnects in an integrated circuit assembly which alleviate problems associated with integrated circuit size and performance.

Structures, systems and methods are provide for multilevel wiring interconnects in an integrated circuit assembly which alleviate problems associated with integrated circuit size and performance. The structures, systems and methods of the present invention include a method for forming multilevel wiring interconnects in an integrated circuit assembly. The method includes forming a number of multilayer metal lines separated by a number of air gaps above a substrate. A silicide layer is

formed on the number of multilayer metal lines. The silicide layer is oxidized. And, a low dielectric constant insulator is deposited to fill a number of interstices created by the number of air gaps between the number of multilayer metal lines. In one embodiment, forming the number of multilayer metal lines includes a first
5 conductor bridge level. In one embodiment, forming a silicide layer on the number of multilayer metal lines includes using a pyrolysis of silane at a temperature of between 300 and 500 degrees Celsius. Also, in one embodiment, a metal layer is formed on the oxidized silicide layer. The metal layer includes a metal layer selected from the group consisting of Aluminum, Chromium, Titanium, and Zirconium. In
10 one embodiment, the metal layer includes a layer of Aluminum oxide.

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or
15 variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used.
20 The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.